IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method of simulating a circuit comprising:

representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the corresponding outputs associated with all of the plurality of identical components; and

symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components.

2. (original) The method defined in Claim 1 wherein the circuit comprises n signals having n states, and further wherein encoding the circuit produces simulation run time data structures asymptotically smaller than n.

3. (original) The method defined in Claim 1 wherein the circuit comprises n signals having 2^n states, and further wherein encoding the circuit produces simulation run time data structures asymptotically close to $\log_2(n)$.

4. (original) The method defined in Claim 1 wherein each input port of the reduced form of the circuit is mapped to an encoded port and each output value is decoded back to a set of values of corresponding outputs of the plurality of identical components, where each value in the set of values corresponds to an output of one of the plurality of identical components.

5. (original) The method defined in Claim 4 wherein each input i of the single instance of the identical component in the reduced form represents the input i for each component in the plurality of identical components.

6. (original) The method defined in Claim 4 wherein each output i of the single instance of the identical component in the reduced form represents the output i for each component in the plurality of identical components.

7. (original) The method defined in Claim 1 wherein each component in the plurality of identical components comprises a plurality of identical subcircuits, and the single instance of the identical component in the reduced form includes a single instance of the identical subcircuit.

8. (original) The method defined in Claim 1 wherein input encoding in the reduced form is generated by applying binary encoding to inputs of the plurality of identical components.

9. (original) The method defined in Claim 1 wherein input encoding in the reduced form is generated by applying ternary encoding to inputs of the plurality of identical components.

10. (original) The method defined in Claim 1 wherein symbolically simulating the reduced form of the circuit is performed using Binary Decision Diagram (BDD).

11. (original) The method defined in Claim 1 wherein the components comprise one or more selected from the group consisting of a net, a port, an array, and a memory.

12. (original) The method defined in Claim 1 wherein at least one of the components comprises at least one signal having a plurality of states.

13. (original) An apparatus of simulating a circuit comprising:

means for representing a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the outputs associated with all of the plurality of identical components; and

means for symbolically simulating the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components.

14. (original) The apparatus defined in Claim 13 wherein the circuit comprises n signals having 2^n states, and further wherein encoding the circuit produces simulation run time data structures asymptotically smaller than n.

15. (currently amended) The apparatus defined in Claim 13 wherein the circuit comprises n signals having 2^n states, and further wherein encoding the circuit produces simulation run time data structures asymptotically close to ~~log(n)~~ $\log_2(n)$.

16. (original) The apparatus defined in Claim 13 wherein each input port of the reduced form of the circuit is mapped to an encoded port and each output value is decoded back to a set of values of outputs of the plurality of identical components,

where each value in the set of values corresponds to an output of one of the plurality of identical components.

17. (original) The apparatus defined in Claim 16 wherein each input i of the single instance of the identical subcircuit in the reduced form of each input i represents the input i for all of the plurality of identical subcircuits.

18. (original) The apparatus defined in Claim 16 wherein each output i of the single instance of the identical component in the reduced form represents the output i for each component in the plurality of identical components.

19. (original) The apparatus defined in Claim 13 wherein each component in the plurality of identical components comprises a plurality of identical subcircuits, and the single instance of the identical component in the reduced form includes a single instance of the identical subcircuit.

20. (original) The apparatus defined in Claim 13 wherein input encoding in the reduced form is generated by applying binary encoding to inputs of the plurality of identical components.

21. (original) The apparatus defined in Claim 13 wherein input encoding in the reduced form is generated by applying ternary encoding to inputs of the plurality of identical components.

22. (original) The apparatus defined in Claim 13 wherein symbolically simulating the reduced form of the circuit is performed using Binary Decision Diagram (BDD).

23. (original) The apparatus defined in Claim 13 wherein the components comprise one or more selected from the group consisting of a net, a port, an array, and a memory.

24. (original) The apparatus defined in Claim 13 wherein at least one of the components comprises at least one signal having a plurality of states.

25. (original) An article of manufacture having one or more recordable media to store executable instructions which, when executed by a processing device, cause the processing device to:

represent a plurality of identical components in a reduced form as a circuit having a single instance of the identical component with encoding for each input of the single instance to represent corresponding inputs to all of the plurality of identical components and decoding for each output port of the single instance to create output ports for the outputs associated with all of the plurality of identical components; and

symbolically simulate the reduced form of the circuit with simulation results being the same as results of symbolically simulating the plurality of identical components.